Integrated Inductors in the Chip-to-Board Interconnect Layer Fabricated Using Solderless Electroplating Bonding

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Abstract — **Integrated inductors are typically formed either on-chip or embedded in the chip package or board. In this work, we explore the possibility of forming inductors in the chip-to-board interconnect layer. The solderless technique of electroplating bonding is used to simultaneously form inductor structures as well as chip-to-board interconnect. The use of the gap between the chip and substrate for inductors not only increases integration density, but also allows large magnetic cross-sectional areas to be achieved. To demonstrate the technology, 3- and 7-turn inductors 500μm in height were fabricated. These inductors showed inductance values of 3.45nH and 10.5nH, respectively. The measured Q-factors of the 3- and 7-turn inductors were 70 and 55 respectively, which agreed very well with modeling results.**

I. INTRODUCTION

The large demand for passive components for consumer products (VCRs, camcorders, pagers, and cellular phones) has led to much work aimed at improving passive component fabrication and packaging. Specifically, the inductor has been a key issue since the three-dimensional configuration of inductors differs greatly from other components (resistors, capacitors and piezoelectric components) in terms of its fabrication. In general, two types (spiral-and solenoid- type) of inductors are typically fabricated for use in integrated systems. In addition to their fabrication, several packaging methods for inductors have been researched. These can be divided roughly into three classes: mounting the inductor on the printed wiring board (PWB) near the chip (the *hybrid mounting* method), mass-forming the inductor on or within the printed wiring board (the *multichip module* (MCM) method), and forming the inductor directly on the semiconductor chip (the *on-chip* method). Hybrid mounting of passive components limits the miniaturization of the whole system board size, potentially leading to cost inefficiencies and introduction of additional parasitics by the required interconnections. On-chip inductor fabrication has been developed for reducing the interconnection parasitics [1-3]. On-chip inductor fabrication usually produces spiral and solenoid inductors. The on-chip spiral-type inductors occupy large areas on the expensive Si substrate. Moreover, stray capacitance effects and, for the case of spiral inductors, the generation of flux perpendicular to the substrate can induce loss if the substrate is lossy (e.g., Si). Solenoid-type on-chip inductors have been fabricated to alleviate the miniaturization problem of spiral inductors, and this approach may be most appropriate when reduction of lead parasitics is the paramount concern. The Multi Chip Module (MCM) approach has been researched with the goal of further miniaturization of the area of the passive component, especially with ceramic substrates [4-6]. In addition, the technology promises to reduce the substrate losses for spiral inductors. However, this approach still poses challenges in that the perpendicular flux still affects the circuitry and other passive components in proximity to the inductor.

In this paper, inductors were fabricated *in the interconnect layer between chip and board.* The rationale behind this choice was (1) to save real estate both on the chip as well as in the package; (2) to reduce parasitics and component/component interaction; and (3) to take advantage of the naturally relatively large gaps between chip and board to produce large magnetic cross-sectional areas (e.g., for increased inductance and Q-factor). Although inductors were chosen as the test vehicle, other large-magnetic-cross-section applications such as antennas may benefit from this approach as well.

Since there is a move to eliminate solder in electronic assembly for environmental reasons, electroplating bonding was utilized as a chip-to-board interlayer formation technique. More information about this technique is given in the next section.

II. DESIGN AND FABRICATION

The schematic of a 3-turn inductor is shown in Figure 1. In this initial work, glass was utilized instead of silicon chips, but the design and fabrication remains unchanged. The primary goal of the design is to obtain very tall inductors in the gap between the two substrates (glass and PWB) using the electroplating bonding packaging interconnection method. The two substrates to be joined

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were a 2.5cm^2 glass substrate (as an initial test) and a 5cm^2 epoxy-glass composite printed wiring board (PWB). High aspect ratio posts were formed on both substrates using an SU-8 process [7], and these posts were subsequently joined using electroplating bonding. The electroplating bonding process was performed by bringing the posts into aligned contact, clamping, and continuing the electroplating process.

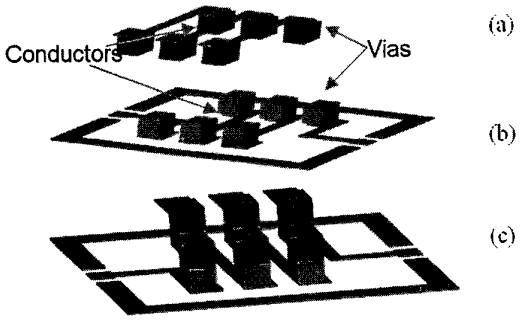


Figure 1. Schematic of 3-turn inductor. (a) upper structures (b) bottom structures before bonding (c) perspective view after electroplating bonding.

The inductance for an ideal solenoid coil can be expressed by equation (1):

$$L = \frac{N^2 \mu w_c h_c}{l_c} \qquad (1)$$

where N is the number of coil turns , μ is the permeability of the core, w_c is the core width, h_c is the core height, and l_c is the core length. In the case of micromachined solenoid inductors, the height of the via is a key parameter for obtaining high inductance and quality (Q) factor. Typically, this via height is limited due to fabrication constraints. However, the interconnect layer approach allows much larger via heights to be achieved. In this study, a 250um high via is formed on each substrate, for a total via height of 500 microns. Also, 3- and 7-turn inductors are fabricated for comparison of the inductance as a function of the number of turns in the coil. The inductor configurations are given in Table I.

The inductor fabrication used photosensitive epoxy (SU8-25, Microchem, Inc,), Cu–electroplating techniques, and the Cu electroplating bonding method. Before fabrication of this kind of inductor, the characterization measurements to be taken after the devices are completed are considered. Because this technique is accomplished by a flip-chip method, the fabricated inductors will be difficult to reach by the measurement probes unless special compensations are introduced. The method that is used in this paper is to remove the upper substrate (glass) by etching the sacrificial layer (2um aluminum) after electroplating bonding to expose the inductors for measurements. In actual application, the removal step would not be required.

The fabrication process of the electroplating bonding inductor is based on a CMOS-compatible plating-through-mold technology, followed by standard surface micromachining. The interlayer inductor fabrication process is described in Figure 2.

Table 1. Configuration of electroplating bonded inductor

Conductor thickness	20um
Via height	250um each
Pitch of turns	100um
Conductor width	50um

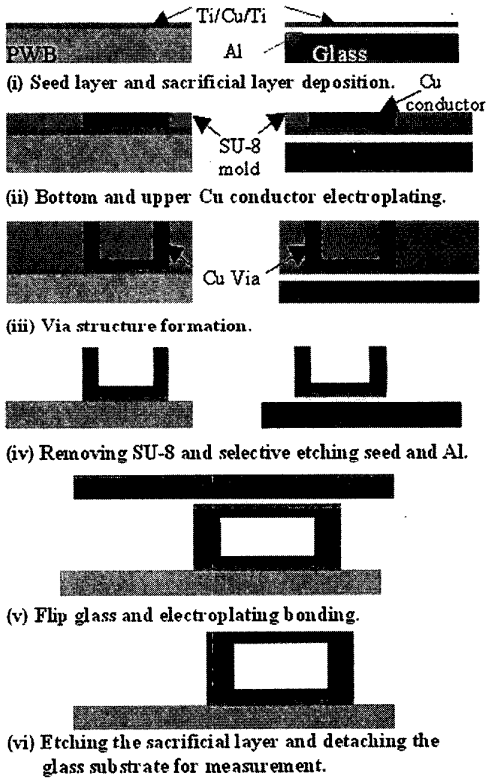


Figure 2. Process schematic of the electroplating bonding inductors

As mentioned above, a 2μm thick aluminum sacrificial layer is sputtered for releasing the glass substrate at the completion of the entire fabrication process. A seed layer of Ti/Cu/Ti (30nm /250nm /30nm) is then deposited as described in Figure 2(i). On this layer, a Cu conductor mold (20μm in thickness) is formed using photosensitive epoxy and patterned using a conventional CMOS photolithography process. The mold is then filled to the top using a Cu electroplating bath as shown in Figure 2 (ii). When the first epoxy mold is filled with electroplated Cu, a thick layer (250μm) of epoxy is spin-cast on the sample again and patterned to create the mold for the via. This via mold is then filled with electroplated Cu. Figure 2(iii) shows the electroplated Cu via which is 250um in height. After the formation of the electroplated Cu structures, the polymers are etched away as shown in Figure 2 (iv). The seed layer and Al sacrificial layer are then selectively etched by metal etchants and RIE, respectively. The flipping of the substrate - which is the same method as the conventional flip chip method - and aligning of the posts on each substrate are performed as shown in Figure 2(v).

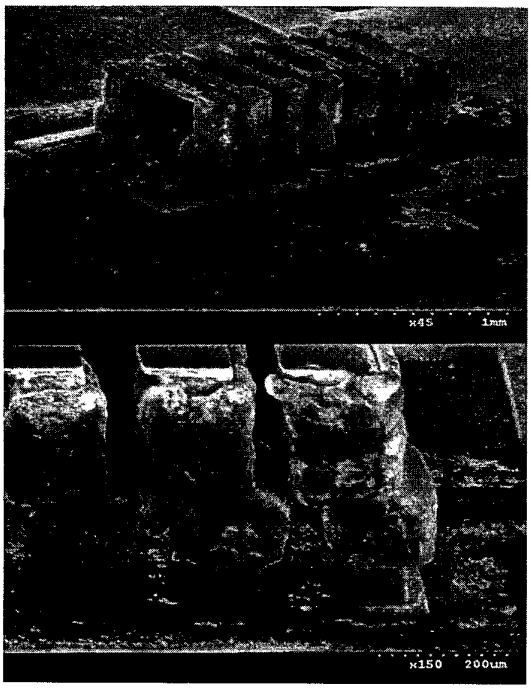


Figure 3. SEM pictures of high aspect ratio inductors fabricated from electroplating bonding technique (after removal of the upper glass substrate). The underlying weave of the epoxy-glass PWB can be seen in the upper picture.

Finally, electroplating bonding is done in a Cu electroplating bath for 30 minutes. For measurement, the glass substrate is released with Al wet etching as shown in Figure 2(vi). Figure 3 shows the SEM pictures of the fabricated structures. The completed electroplating bonded inductors have a height of 500um.

III. Characterization and Modeling

The quality factor (Q) and self-resonance frequency (SRF) of inductors were analyzed using the usual lumped element circuit model for a two-port inductor shown in Figure 4 [8]. The model consists of an ideal inductor L in series with a resistor R to account for the conductor loss. The dielectric loss and the parasitic capacitance are represented by R_P and C_P, respectively. C_P results from the substrate capacitance and coupling capacitance between turns.

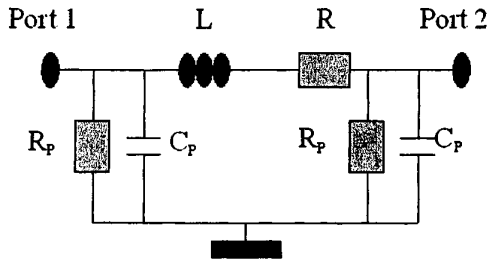
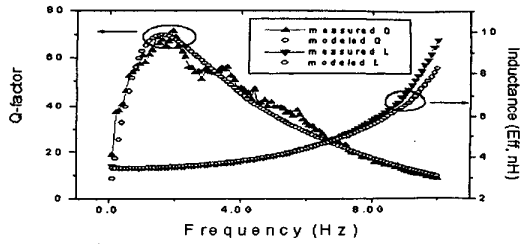


Figure 4. Two-port inductor electrical model used for the performance optimization.

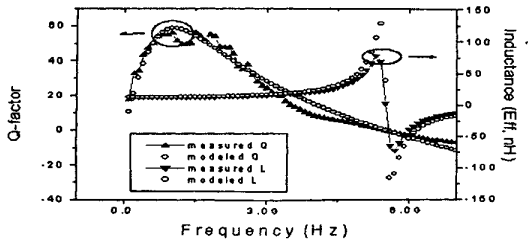
The S-parameters of the two-port inductor were measured using an HP8517 network analyzer and transformed into effective inductance (L_{Eff}) and Q-factor using the software package HP ADS.

Figure 5 shows measured and modeled effective inductance and the Q-factor of the 3- and 7-turn inductors, while Table 2 summarizes performance of 3- and 7-turn inductors.

The extracted lumped element values for both 3- and 7-turn inductors are shown in Table 3. The behavior of the inductor over the frequency ranges of interest is well described by Figure 4 as shown by the close agreement between measured and modeled curves in Figure 5.



(a)



(b)

Figure 5. Measured and modeled L_{EFF} and Q of (a) 3-turn and (b) 7-turn inductors.

Table 2. Inductor performance.

No. of turns	L (nH)	Q_{MAX}	SRF(GHz)
3	3.45	71@2.0GHz	12
7	10.5	56@1.5GHz	5.5

Table 3. Summary of extracted circuit parameters.

No. of turns	L (nH)	R (Ω)	C_P (fF)	R_P (kΩ)
3	3.45	0.25	43	5
7	10.4	0.6	78	9

IV. CONCLUSION

A high inductance, high quality factor, and packaging compatible electroplating bonded inductor for RF systems has been proposed and demonstrated. This technique is compatible with standard back-end CMOS processing and combines electroplating bonding of copper posts with surface micromachining technology. Fabricated structures have demonstrated that the electroplating bonding inductor can lead to real-estate savings on silicon or PWB substrates since the inductor was formed in the gap between substrates. Also, this technique produced a packaged system with Cu interconnection for improved electrical and mechanical characteristics. The characteristics of the inductor were measured and simulated. Because these structures have a large flux area, the electroplating bonded inductors produced high inductances of 3.45nH and 10.4nH in 3- and 7-turn coils, respectively. High Q-factors of 71 and 55 were also obtained from the 3- and 7-turn structures, respectively. Although inductors were chosen as the test vehicle, other large-magnetic-cross-section applications such as antennas may benefit from this approach as well.

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